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(54) Insulated gate field-effect transistors

(57) A field-effect transistor such as a LDMOS or a LIGBT having first and second electrical terminals, at least a first pn junction (2/6) adjacent the first terminal (S) and a second pn junction (5/7,5/8) adjacent the second terminal (D), wherein at least one further pn junction (5/6) extends between said first and second pn junctions so as to be transverse thereto. At least one gate terminal (G1) is disposed over a doped region (2) adjoining the first pn junction on the opposite side to that of the further pn junction with respect to the first pn junction. A second gate terminal may be disposed over a doped region (8) adjoining the second pn junction on the opposite side to that of the further pn junction with respect to the second pn junction. The double-gate devices are formed of a pair of associated, complementary LDMOS devices which may operate in unipolar (MOSFET) modes with any one of the gates active or in bipolar (IGBT) mode with both gates active, or of a pair of associated, complementary LIGBT devices. SOI substrates may furthermore be used.

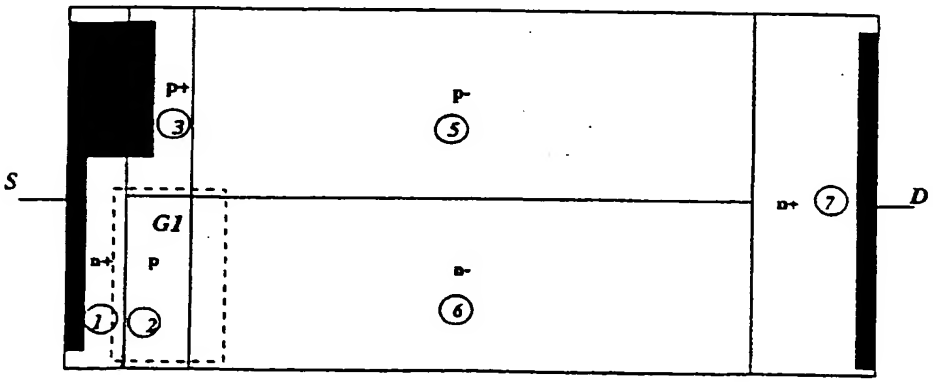


Figure 6:

EP 1 026 750 A1

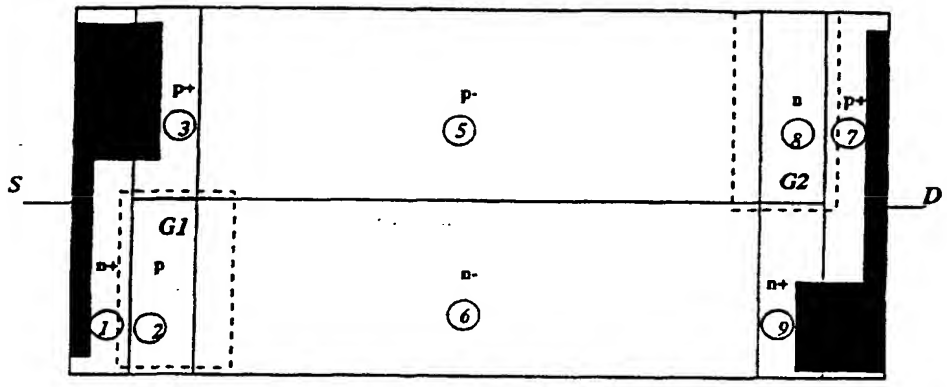


Figure 9

Description

[0001] This invention relates to semiconductor devices. In particular, it relates to improvements in high voltage, large current, devices.

[0002] It has been a long desired goal in the field of semiconductor device design and manufacture to provide semiconductor devices which are capable to controlling high voltages and large currents. In particular, it has long been desirable to provide semiconductor devices which can withstand high voltages being applied across them without breaking down, and which can handle large currents during operation.

[0003] The present invention seeks to provide devices which meet this goal.

[0004] According to the present invention there is provided a semiconductor device having first and second electrical terminals, the device comprising:

at least one n/p or p/n first junction adjacent the first terminal;
at least one of the other of a p/n or n/p second junction adjacent the second terminal;
at least one n/p or p/n junction disposed between the first and second junctions and arranged to be transverse thereto; and
at least one gate terminal in contact with the p or n doped region of the first junction or the n or p doped region of the second junction.

[0005] The semiconductor device may have more than one gate, the gates arranged to control the flow of carriers through the device. The gates may be formed from metal or polysilicon on an insulating layer.

[0006] The device may be formed on a substrate consisting of an oxide layer on a silicon substrate or, alternatively, upon a p- or n- doped silicon substrate.

[0007] The device may be formed as part of an integrated circuit.

[0008] One example of the present invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a schematic perspective diagram showing a diode employing principles employed in the present invention;
Figure 2 is a schematic perspective diagram of the diode of figure 1 formed on a different substrate;
Figures 3A and 3B are schematic diagrams showing conventional diodes and the electric fields and potential distribution associated therewith during reverse voltage bias;
Figure 4 shows representations corresponding to those in figures 3A and 3B but for the diode of figure 1;
Figure 5 is a schematic perspective view of an example of the present invention;
Figure 6 is a plan view of the device of figure 5;
Figure 7 is a plan view of the complementary device of figure 6;
Figure 8 is a schematic perspective view of an adaptation of the device of figure 5;
Figure 9 is a plan view of the device of figure 8;
Figure 10 is a graph showing the output characteristics of the device of figures 8 and 9;
Figure 11 is a graph showing the doping levels and electron and hole concentrations of the device of figures 8 and 9 during operation;
Figure 12 is a plan view of the device of figures 8 and 9 showing the depletion region during turn-off of the device;
Figure 13 is a plan view of a further example of the present invention;
Figure 14 is a plan view of the example of figure 13 showing its depletion region during turn-off;
Figure 15 is a plan view of a further example of the present invention;
Figure 16 is a plan view showing the depletion region of the example of figure 15 during turn-off; and
Figures 17 to 23 are plan views of further examples of the present invention.

[0009] A basic junction arrangement of the type employed in the present invention is shown in figure 1. The arrangement of figure 1 is a diode having a cathode K and anode A. The diode is based upon alternate low-doped n and p silicon layers placed on a silicon on insulation (SOI) substrate. Figure 2 shows a similar arrangement to that of figure 1, but formed on a lowly doped p- substrate, employing junction isolation (JI) technology for integrated circuits. In the arrangement of figure 2, the substrate is connected to the anode A via a p- doped layer.

[0010] Referring to figure 1, the diode 10 has three physical junctions, the first being the n+/p- junction adjacent the cathode K, the second p+n- junction adjacent the anode A, and the third the p-/n- junction transverse to the first and second junctions.

[0011] Figures 3A and 3B show the potential in conventional power diodes in breakdown mode, when a high voltage is applied to its cathode, indicating that there is a peak in the electric field at one side of each of the devices which then decreases linearly.

[0012] Referring to figure 4, the characteristics of an arrangement of the present invention are very different. Because of the transverse junction, and particularly central continuity of potential across the transverse junction when this is fully depleted, the lines are drawn from anode A and cathode K towards the centre of the diode, leading to a uniform distribution in both the central n- and p- regions. The arrangement of the diode of figures 1 and 2 therefore realises a breakdown voltage which is much larger (in this example approximately 760 volts) than that of an equivalent conventional diode.

[0013] Figure 5 is a schematic diagram showing a first example of the present invention. This example shows

an SOI arrangement with a substrate, but a similar arrangement on a JI substrate could be provided. In this example, a gate G1 is provided to give a MOSFET arrangement. Figure 6 shows a plan view of the arrangement of figure 5. In its off state, during forward voltage blocking the action of the three junctions (between regions 2/6 7/5. and 5/6). is the same as in the diode of figure 1 In the on state, a potential higher than a threshold voltage is applied to the gate G1 with respect to the source S. allowing electron flow from the n+ region (region 1) through the channel formed in the p layer (region 2) beneath the gate G1, n-layer (region 6). to the n+ region (region 7) and the drain D. Figure 7 shows a device complementary to that of figure 6, with a gate G2 above an n- doped region.

[0014] Figures 8 and 9 show an adaptation of the device of figure 5. in which two gates, G1, G2 are provided. The operation of this example in the off-state is the same as previous examples, but in its on-state this example has three operating modes, two which are unipolar, and one which is bipolar. The operation of the example of figure 8 is such that the current density passing through the device in the on state is increased. because the p-layer is used to transport holes from the drain to the source as electrons are transported in the opposite direction through the n- layer.

[0015] Referring to figure 9. in a first on mode, when only the gate G1 is active, a channel is induced at the surface of the p layer, allowing transportation of electrons from the n+ source S onto the drain D.

[0016] In a second mode, when only the gate G2 is active. holes are transported from the p+ layer via the channel formed in the n layer through the p- drift layer, via the p+ layer to the drain D.

[0017] These two operations are similar to that of the examples of figures 6 and 7.

[0018] In the bipolar mode, in which both gates G1, G2 are active and an inversion condition is obtained for the regions beneath each of the gates G1, G2. Initially, holes and electrons flow without interfering, but once the transverse p-/n- junction becomes forward biased, injection of minority carriers takes place across this junction. When a high level of injection is established and a plasma of mobile carriers is formed, the on-state resistance of the device decreases drastically. The voltage level at which this forward biasing occurs depends upon the potential distribution in the layers forming the transverse junction. which is in turn influenced by the thickness and doping of the regions of the device, together with the oxide thickness in the case of an SOI structure.

[0019] Figure 10 shows the output on state characteristics for the device of figures 8 and 9 for the cases (a), when both gates are active. (b), when only gate G1 is active, and (c). when only gate G2 is active. From figure 11 it can be seen that the levels of electrons (ii) and holes (iii) in the two regions forming the transverse junction are well above their actual doping concentrations (i), indicating conductivity modulation.

[0020] With this arrangement. unlike in conventional power devices, both the source and drain junctions are shorted, (i.e. the source electrode contacts the n+ region (1) and the p+ region (3) and thus shorts the n+/p junction, and the drain electrode contacts the p+ region (7) and the n+ region (9) and thus shorts the p+/n junction) resulting in very fast switching as, during turn off, the excess charge can be eliminated via these shorts.

[0021] The device is turned off by decreasing the relative potentials applied to the two gates G1, G2 below a threshold voltage necessary to form channels in the region below the two gates. The three junctions referred to previously then start a reverse recovery and the depletion region expands, as shown in figure 12. The electric field drives out both electrons and holes. Turn-off is complete when the depletion region covers fully the two regions forming the transverse junction.

[0022] Figure 13 shows a further example of the present invention. This example of the present invention is a single gate LIGBT, which has the advantage over the single gate example of figure 5 that it has a reduced on-state resistance. Again, the off-state action of the device of figure 13 is generally the same as with the example of figure 1. In the on-state, when G1 has a voltage applied thereto, and there is an appropriate voltage differential between anode A and cathode K, an inversion layer forms in the region under the gate G1, allowing electron flow. Because the junction between regions 7 and 8 is forward biased in such a situation, holes are injected across this junction into the regions forming the transverse junction. Such holes can then pass via several routes through to the cathode. The presence of holes in both of the regions forming the transverse junction will ensure conductivity modulation in both of these regions, but the n- region will be more highly modulated because of enhanced injection of electrons from the cathode.

[0023] Turn-off of the example of figure 13 is based upon the reverse recovery of the three fundamental junctions. Figure 14 shows the depletion region during turnoff. Again, the electric field and expansion of the depletion region drive holes out of the device via the routes indicated. Any remaining excess charge is eliminated through recombination.

[0024] If a reduced turn-off time is required for the device of figure 13, then an arrangement of the type shown in figure 15 can be employed. This has an arrangement in which the p+ anode region (7) is shorted to the n doped region (2) via the adjacent n+ region (3). During turn-off both electrons and holes are driven out via the route indicated in figure 16. increasing the speed of the device during turn-off. It will be appreciated that, however, this arrangement has higher on-state resistance.

[0025] Figures 17 and 18 show devices complementary to those shown in figures 13 through 16.

[0026] Figure 19 shows a two gate version of arrangement of figures 13 and 15. As with previous examples, the off-state characteristic operates in accordance with

the principles of the arrangement of figure 1, and the on-state has three operations

[0027] In the on-state, when a potential is applied to G1 to generate a potential difference between gate G1 and cathode K that is greater than the MOS threshold voltage a channel is formed in the region beneath the gate G1 This allows electron flow which generates a forward bias at the junction between regions 7 and 9 adjacent to the anode A. This forward biasing results in an injection of holes from region 7 into regions 9 and 6. Again conductivity modulation is generated, resulting in a low on-resistance. It should be noted that during this operation the junction between regions 7 and 10 may also become forward biased, injecting holes from region 7 to region 10 via region 5 and then transversely down through regions 3 and 4 to region 2 and the cathode. When only gate G2 has a potential applied the operation is similar and symmetrical to that when a potential is applied only to gate G1.

[0028] The device is designed, however, to have a normal operation which involves a potential being applied to both gates G1 and G2. This leads to a high degree of modulation and extremely low on-state resistance Holes are injected via the junction between regions 7 and 9. Electrons are injected via the junction between regions 1 and 3, resulting in the low on-state resistance. The device is switched off by removing the potential voltage applied to gates G1 and G2, generating a depletion region as shown in figure 20 The shorts in the anode A and cathode K mean that the device of this example is very fast and has very short switching times.

[0029] Figure 21 shows a further example of the present invention in which the device with two gates G1, G2 is provided. This device is generally a combination of the example of figure 5 and figure 13. The off-state operation of this device is generally similar to that of previous examples. Again, the on-state operation is of three different types.

[0030] Firstly, if a potential is applied only to gate G2, then the device has a unipolar transport of holes from the anode A via a channel formed by the potential on the gate G2 in the region beneath the gate G2. The holes are then transported through the p- region 5 and the p+ region 3 to the cathode K. If only gate G1 is active, then the device allows electrons to flow from the cathode through the region under gate G1 and through the n- region 6 to the anode A. In this case, the on-state resistance will be lower than when only gate G2 is active, but there is a snap-back characteristic which may be undesirable in certain applications

[0031] If potentials are applied to both gates G1, G2 then the resistance in the on-state is reduced considerably and there is no snap-back characteristic.

[0032] Figure 22 shows the depletion region of the device of figure 21 as the device is being made inactive by removing potentials from gate G1 and G2. The turn-off operation of this example is similar to those of previous examples.

[0033] Figure 23 shows a device complementary to that of figure 21.

Claims

1. A semiconductor device having first and second electrical terminals, the device comprising:

   at least one n/p or p/n first junction adjacent the first terminal;
   at least one of the other of a p/n or n/p second junction adjacent the second terminal;
   at least one n/p or p/n junction disposed between the first and second junctions and arranged to be transverse thereto; and
   at least one gate terminal in contact with the p or n doped region of the first junction or the n or p doped region of the second junction;
   wherein the device is arranged to operate as a MOSFET or as an LIGBT.

2. A device according to claim 1, wherein the device has more than one gate, each of the gates arranged to control the flow of carriers through the device, and arranged to operate as a double gated LIGBT.

3. A device according to claim 2, arranged to operate both as a LIGBT and a MOSFET.

4. A device according to any preceding claim, wherein device is formed on a substrate consisting of an oxide layer on a silicon substrate.

5. A device according to any of claims 1 to 3, wherein the device is formed on a p- or n- doped silicon substrate.

6. A device according to any preceding claim, formed as part of an integrated circuit.

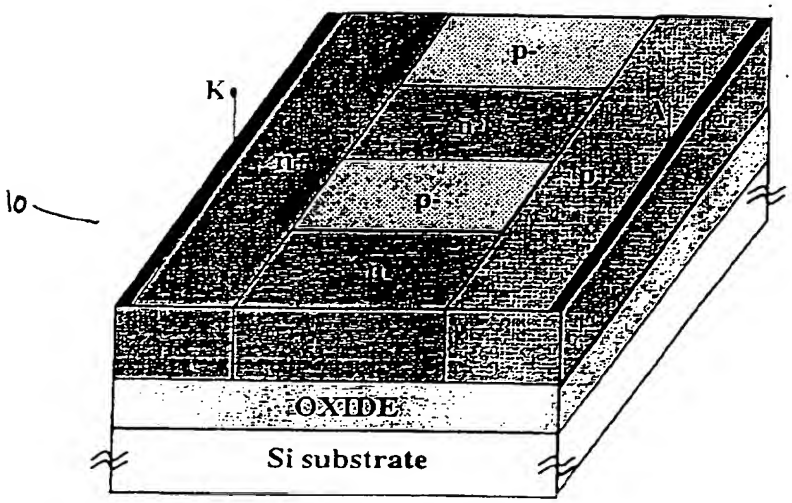


Figure 1:

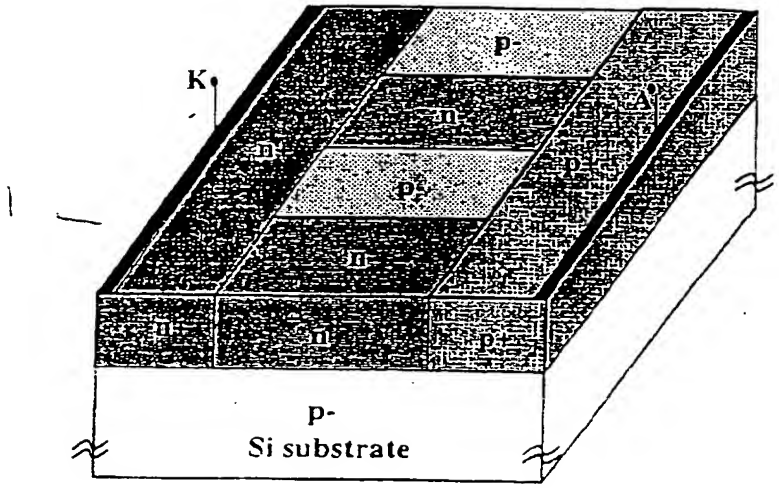
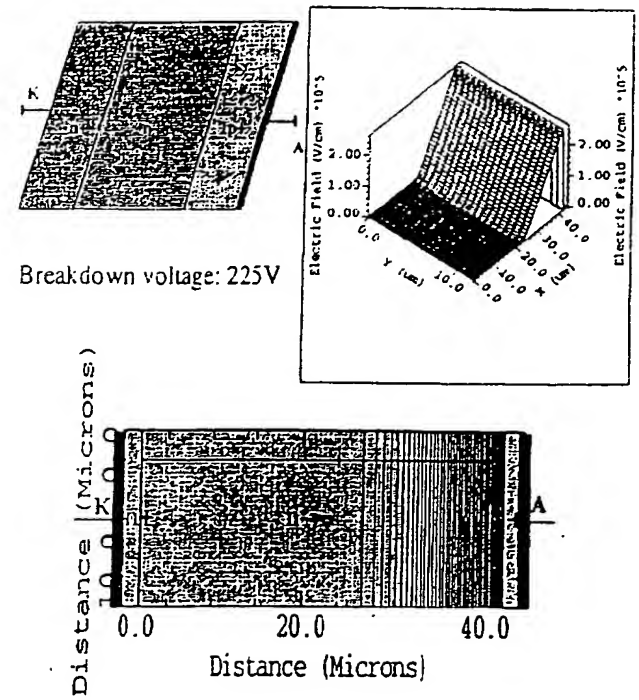
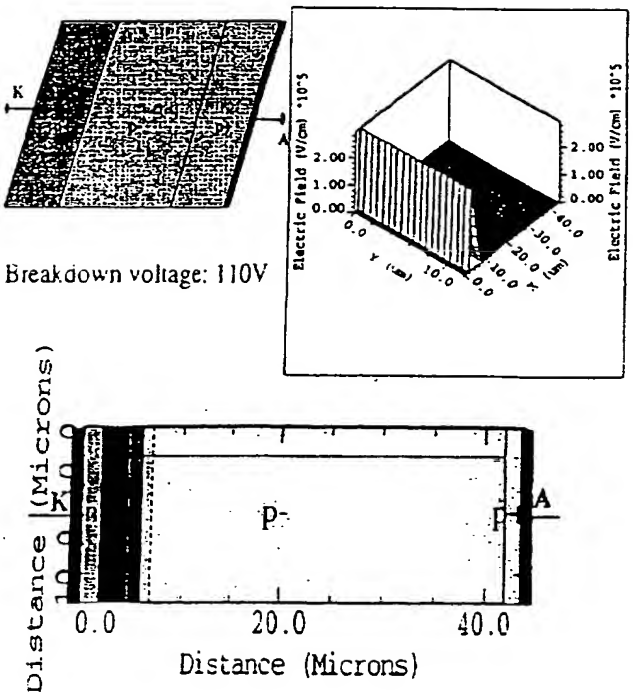


Figure 2:



(a)



(b)

Figure 3:

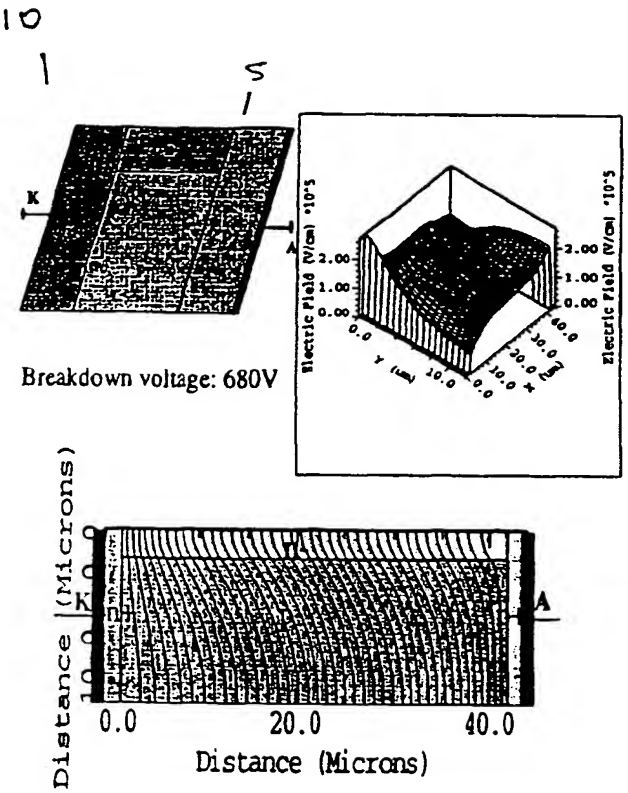


Figure 4:

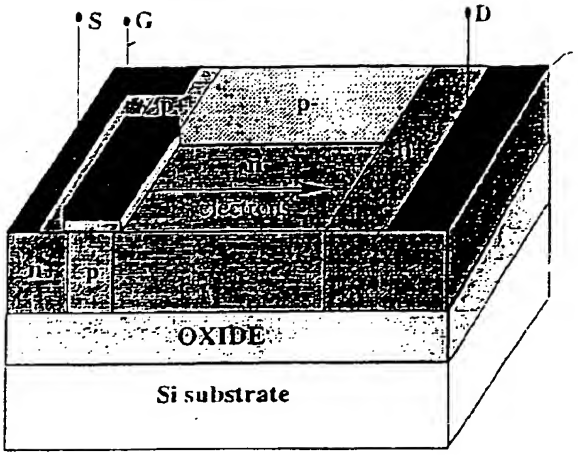


Figure 5:

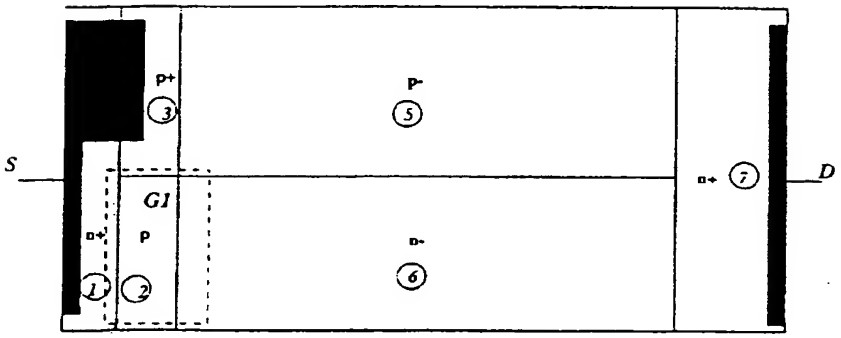


Figure 6:

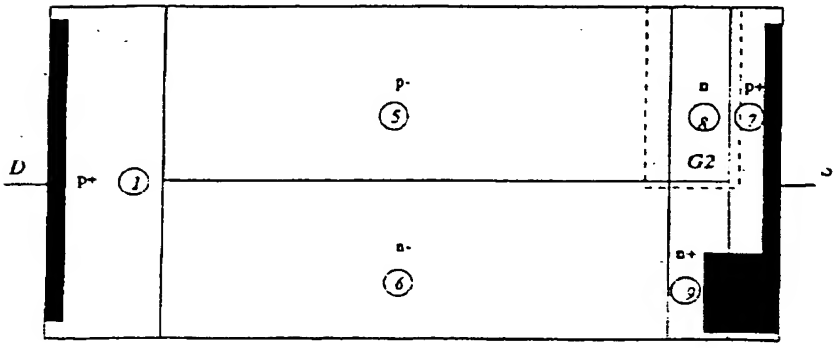


Figure 7

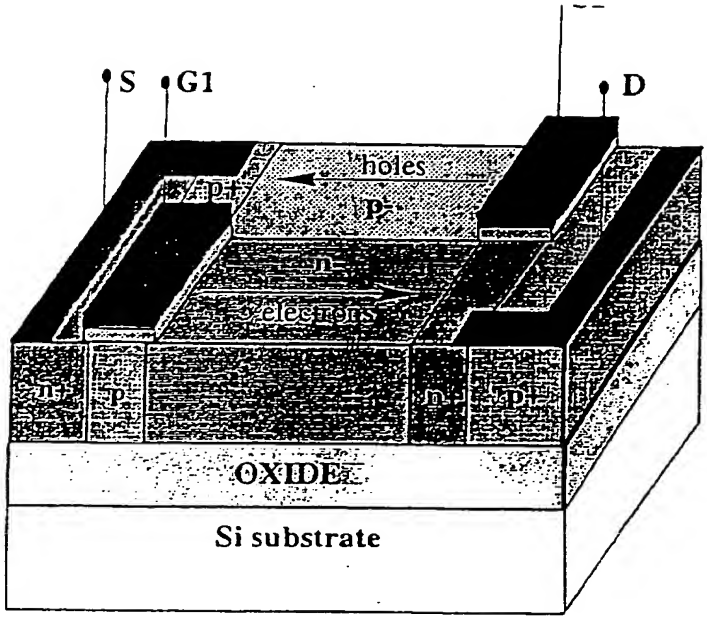


Figure 8.

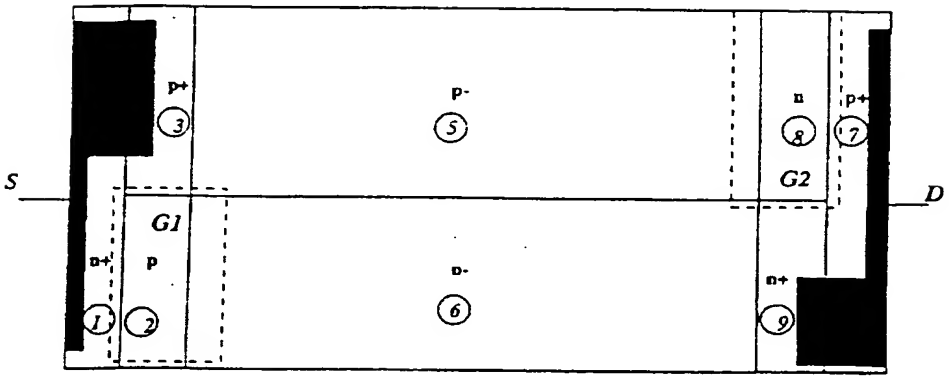


Figure 9

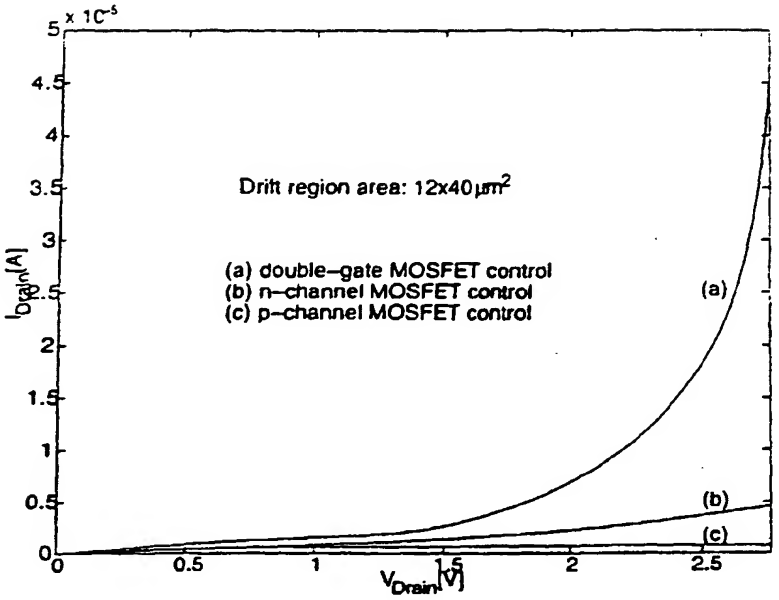
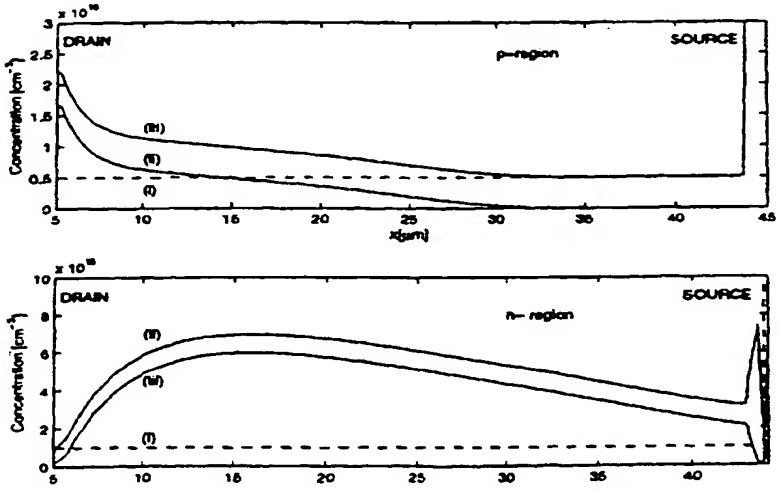


Figure 10



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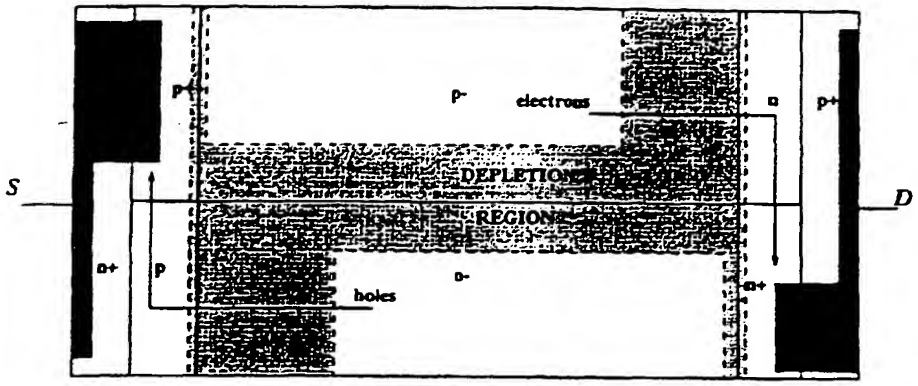

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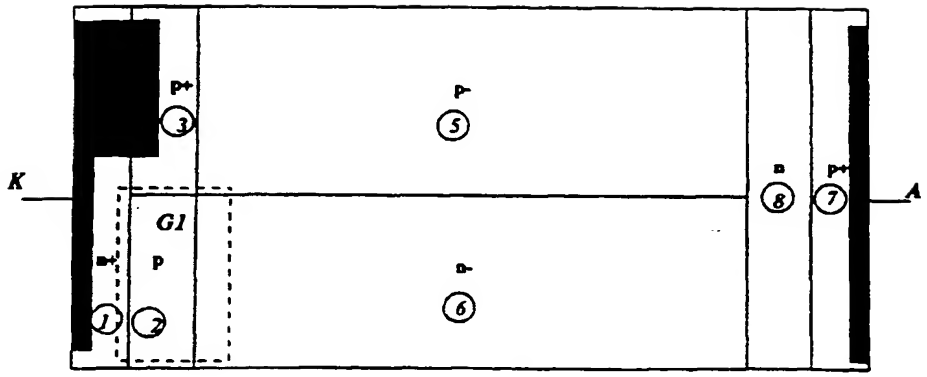


Figure 13

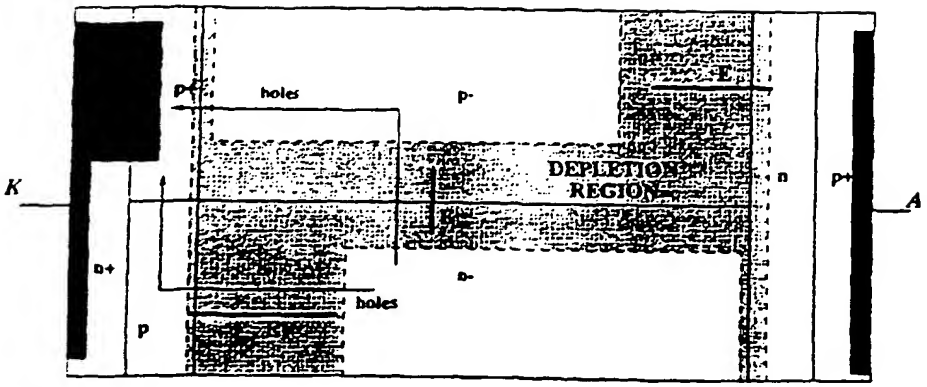


Figure 14:

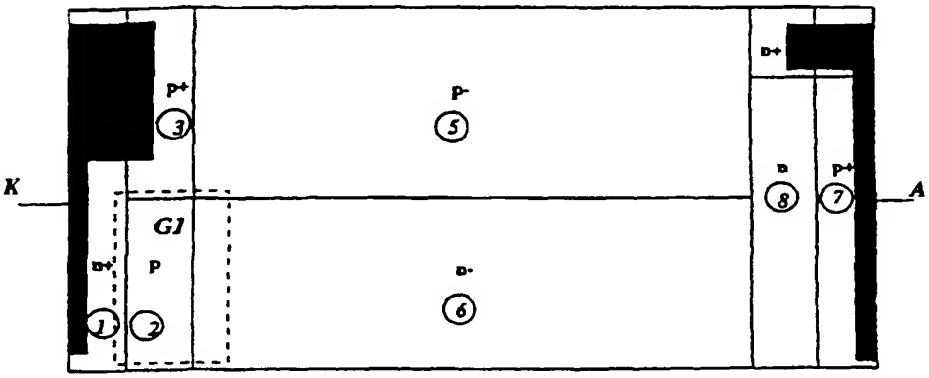
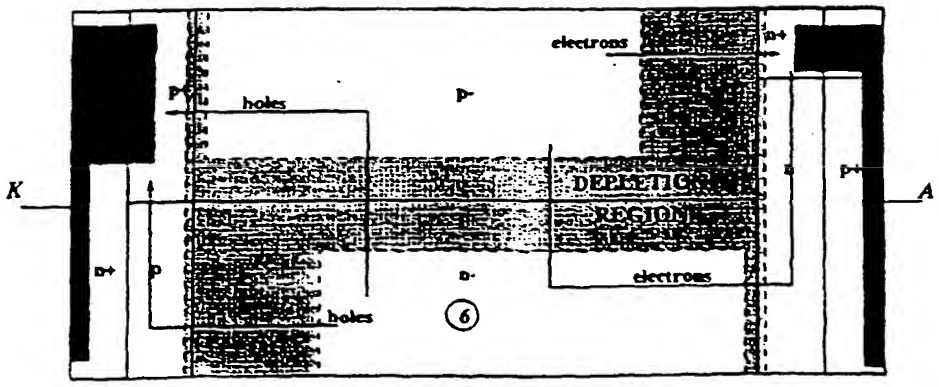


Figure 15.



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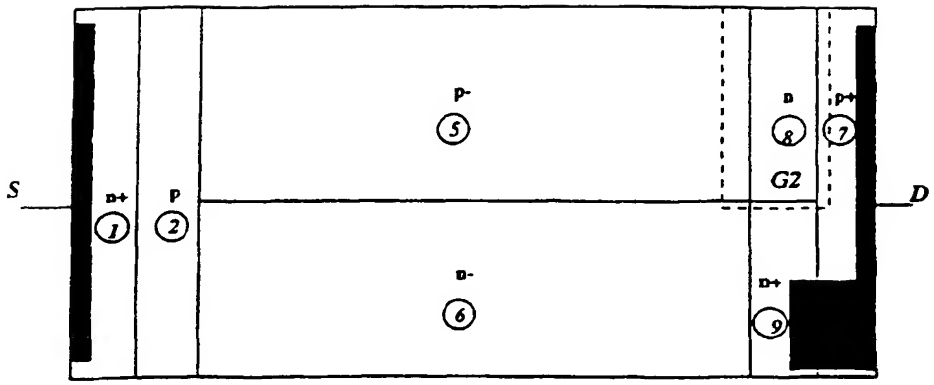

Figure 17

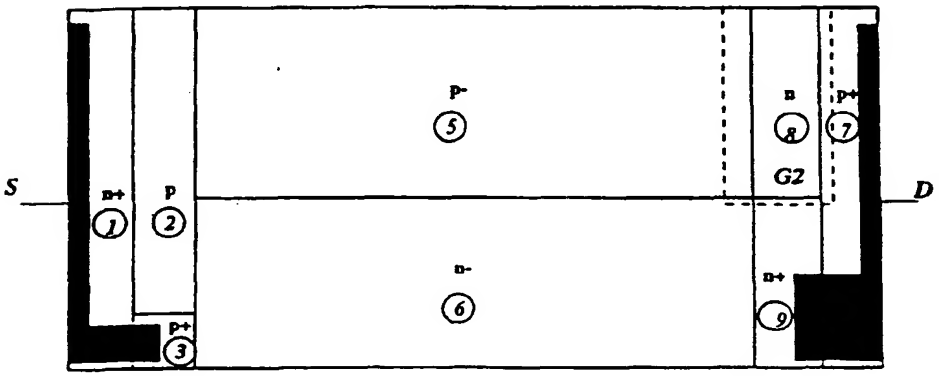

Figure 18

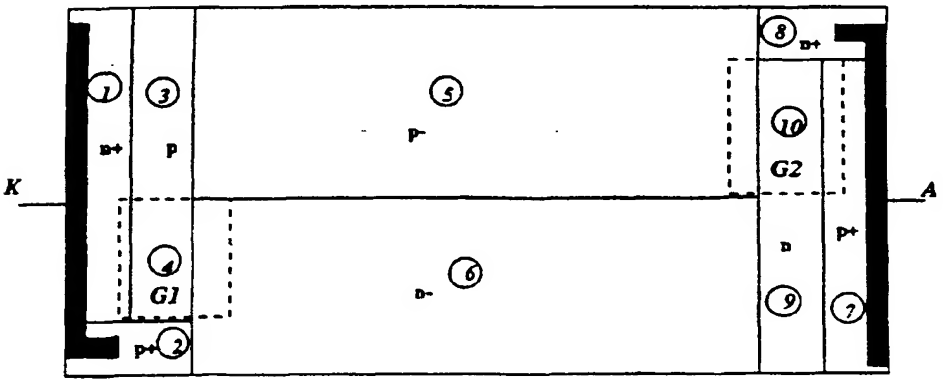

Figure 19

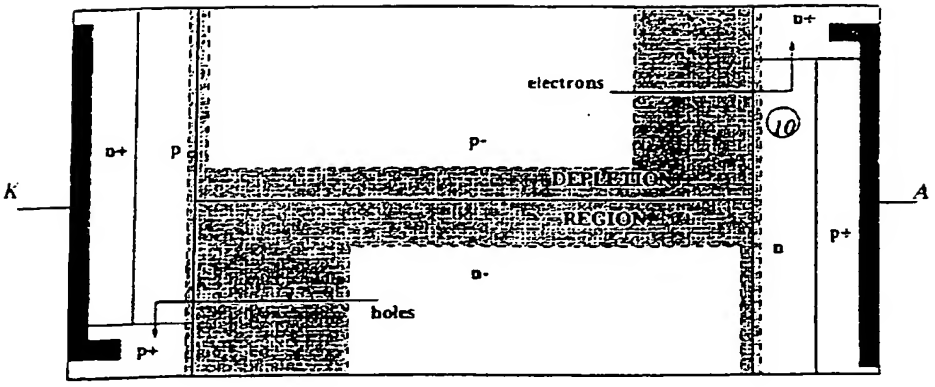

Figure 20:

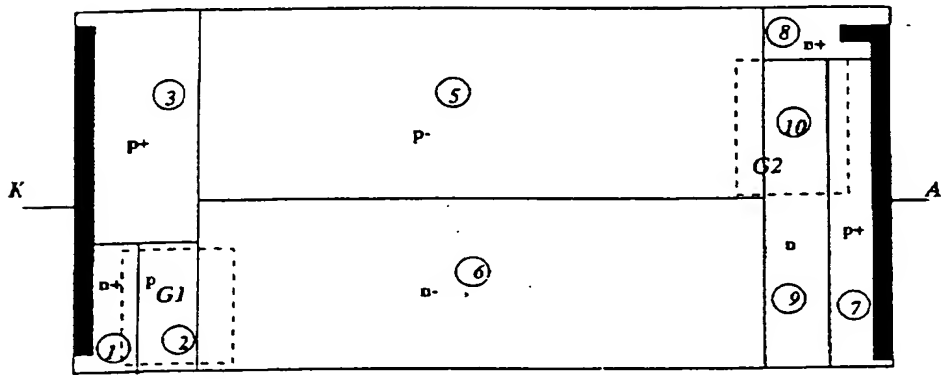

Figure 21:

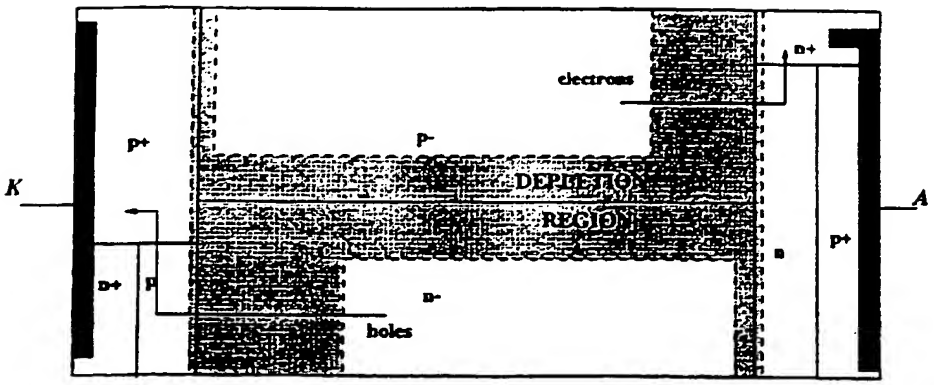

Figure 22:

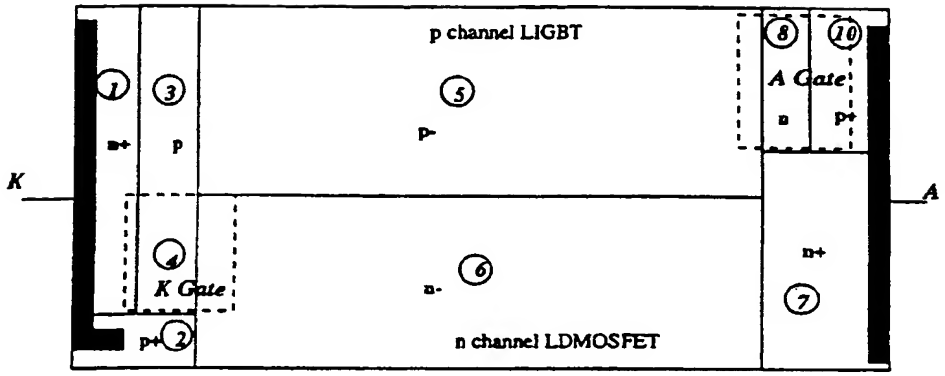

Figure 23:

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 6204

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	UDREA F ET AL: "A new class of lateral power devices for HVIC's based on the 3D RESURF concept" PROCEEDINGS OF THE 1998 BIPOLAR/BICMOS CIRCUITS AND TECHNOLOGY MEETING (CAT. NO.98CH36198), MINNEAPOLIS, MN, USA, 27-29 SEPTEMBER 1998, pages 187-190, XP002125155 1998, Piscataway, NJ, USA, IEEE, USA ISBN: 0-7803-4497-9 * paragraph 3; figure 4 *	1-6	H01L29/78 H01L29/739
X	UDREA F ET AL: "3D RESURF double-gate MOSFET: A revolutionary power device concept" ELECTRONICS LETTERS, vol. 34, no. 8, 16 April 1998 (1998-04-16), pages 808-809, XP000781474 IEE, STEVENAGE, GB ISSN: 0013-5194 * the whole document *	1-6	
X	UDREA F ET AL: "The 3D RESURF junction" 1998 INTERNATIONAL SEMICONDUCTOR CONFERENCE, CAS'98 PROCEEDINGS (CAT. NO.98TH8351), SINAIA, ROMANIA, 6-10 OCTOBER 1998, vol. 1, pages 141-144, XP002125156 1998, New York, NY, USA, IEEE, USA ISBN: 0-7803-4432-4 * paragraph 4; figure 4(a) *	1-6	
X	GB 2 309 336 A (FUJI ELECTRIC CO LTD) 23 July 1997 (1997-07-23) * page 26, line 14 - page 35, line 9; figures 6A-6C,7A-7C *	1,4-6	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)
H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	9 December 1999	Morvan, D

CATEGORY OF CITED DOCUMENTS
X : particularly relevant if taken alone
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